UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/068,957	02/11/2002	Takaaki Ono	111932	2382

25944 7590 07/15/2003

OLIFF & BERRIDGE, PLC
P.O. BOX 19928
ALEXANDRIA, VA 22320

EXAMINER	
KRUER, KEVIN R	
ART UNIT	PAPER NUMBER
1773	7

DATE MAILED: 07/15/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/068,957	ONO ET AL.	
	Examiner	Art Unit	
	Kevin R Kruer	1773	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on *02 May 2003* .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-8* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-8* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

DETAILED ACTION

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

1. Claims 1-6 are rejected under 35 U.S.C. 103(a) as being unpatentable over Gause et al (US 3,895,198) in view of Voroba (US 3,616,984). Gause teaches a metal clad laminate constructed by sandwiching a resin impregnated core paper between epoxy resin impregnated woven glass fabric sheets (herein relied upon to read on the claimed "resist") (abstract). The cellulose papers may be treated with phenolic resin (col 6, line 39+). The metal cladding may comprise copper (col 7, line 20). The laminate may be used a printed circuit board (abstract).

Gause does not teach that the resists should not be applied to areas "adapted to have the terminals of electronic components soldered on the copper foils. However, Voroba teaches that printed circuit boards typically have numerous components, such as integrated circuit modules, transistors, resistors, capacitors, and the like mounted thereon. The leads of such components are mechanically and electrically connected to the board by soldering. The leads are projected through holes in the board and then soldered thereto (col 1, lines 10+). Thus, it would have been obvious to put holes in the

printed circuit board taught in Gause (including the resists layers) in order to provide areas to which components may be soldered.

NOTE: the examiner takes the position that such "through holes" in the resist layer would read on the claimed "areas adapted to have the terminals of electronic components soldered on the copper foils."

2. Claims 7 and 8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Gause et al (US 3,895,198) in view of Voroba (US 3,616,984), as applied to claims 1-6 above, and further in view of Huang et al (US 5,062,896). Gause in view of Voroba are relied upon as above.. Specifically, Gause in view of Voroba teaches that components should be soldered to a printed circuit board through holes in the board. Neither reference teaches that the solder should be lead free. However, Huang teaches that lead containing solders are environmentally undesirable in the connection of components to printed circuit boards (col 1, lines 13+). Therefore, it would have been obvious to one of ordinary skill in the art to utilize a lead free solder for the purpose of protecting the environment.

3. Claims 1-4 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nomura (US 4,029,845) in view of Voroba (US 3,616,984). Nomura teaches a base board for a printed circuit prepared from a laminate comprising at least one sheet of prepeg comprising a thermosetting resin as impregnate and a layer of composition comprising a semi-cured thermosetting resin and a nitrile rubber (herein relied upon to read on the claimed "resist") on both sides of said prepeg layer (abstract). The prepeg

comprises a paper impregnated with a phenolic resin (col 3, lines 18+). A copper foil may be applied to said base board (col 1, lines 29+).

Nomura does not teach that the resists should not be applied to areas "adapted to have the terminals of electronic components soldered on the copper foils. However, Voroba teaches that printed circuit boards typically have numerous components, such as integrated circuit modules, transistors, resistors, capacitors, and the like mounted thereon. The leads of such components are mechanically and electrically connected to the board by soldering. The leads are projected through holes in the board and then soldered thereto (col 1, lines 10+). Thus, it would have been obvious to put holes in the printed circuit board taught in Nomura (including the resists layers) in order to provide areas to which components may be soldered.

NOTE: the examiner takes the position that such "through holes" in the resist layer would read on the claimed "areas adapted to have the terminals of electronic components soldered on the copper foils."

4. Claims 7 and 8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nomura (US 4,029,845) in view of Voroba (US 3,616,984), as applied to claims 1-4 above, and further in view of Huang et al (US 5,062,896). Nomura in view of Voroba are relied upon as above. Specifically, Nomura in view of Voroba teaches that components should be soldered to a printed circuit board through holes in the board. Neither reference teaches that the solder should be lead free. However, Huang teaches that lead containing solders are environmentally undesirable in the connection of components to printed circuit boards (col 1, lines 13+). Therefore, it would have been

obvious to one of ordinary skill in the art to utilize a lead free solder for the purpose of protecting the environment.

Response to Arguments

Applicant's arguments with respect to claims 1 and 2 have been considered but are moot in view of the new ground(s) of rejection.

With respect to Nomura and Gause, Applicant argues that neither reference teaches that the resist should be removed at areas adapted to have the terminals of electronic components soldered on the copper foils." The examiner agrees with Applicant's interpretation, and has applied the teachings of Voroba to compensate for said defeciency.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of

the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Kevin R Kruer whose telephone number is 703-305-0025. The examiner can normally be reached on Monday-Friday from 7:00a.m. to 4:00p.m.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Paul Thibodeau, can be reached on (703) 308-2367. The fax phone number for the organization where this application or proceeding is assigned is 703-305-5408.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0661.

K-R K—

KRK

Paul Thibodeau
Supervisory Patent Examiner
Technology Center 1700